

## WHAT IS CLAIMED IS:

- 1 1. A semiconductor device comprising:
  - 2 a RAM for use in processing incorporated in
  - 3 a data processing system and to be tested;
  - 4 a built-in self test circuit for making a
  - 5 built-in self test on said RAM for use in processing;
  - 6 and
  - 7 a RAM for tester for storing results of said
  - 8 built-in self test on said RAM for use in processing
  - 9 made by said built-in self test circuit so that the
  - 10 results of said built-in self test can be read out by
  - 11 an external tester;
  - 12 a RAM having a data read-out margin greater
  - 13 than a data read-out margin of said RAM for use in
  - 14 processing being used as said RAM for tester.
- 1 2. A semiconductor device comprising:
  - 2 a plurality of RAMs for use in processing
  - 3 incorporated in a data processing system and to be
  - 4 tested; and
  - 5 a built-in self test circuit for making a
  - 6 built-in self test on said RAMs for use in processing;
  - 7 when said built-in self test circuit makes
  - 8 the built-in self test on a part of said plural RAMs
  - 9 for use in processing, a RAM for use in processing,
  - 10 which is not to be tested in said built-in self test,

11 being used as a RAM for tester which stores results  
12 of said built-in self test on said RAM(s) for use in  
13 processing made by said built-in self test circuit so  
14 that the results of said built-in self test can be read  
15 out by an external tester.

1 3. The semiconductor device according to claim 2,  
2 wherein each of said plural RAMs for use in processing  
3 comprises a margin widening means for increasing a bit  
4 line amplitude at the time of a start of a sense  
5 amplifier of said RAM to widen a data read-out margin.

1 4. The semiconductor device according to claim 3,  
2 wherein said margin widening means comprises a delay  
3 circuit for gradually delaying a start timing of said  
4 sense amplifier according to a signal fed from the  
5 outside.

1 5. The semiconductor device according to claim 3,  
2 wherein said margin widening means changes a setting  
3 so that a data read-out margin of a RAM used as a RAM  
4 for tester among said plural RAMs for use in processing  
5 is greater than a data read-out margin of a RAM for  
6 use in processing to be tested in said built-in self  
7 test.

1 6. The semiconductor device according to claim 4,

2 wherein said margin widening means changes a setting  
3 so that a data read-out margin of a RAM used as a RAM  
4 for tester among said plural RAMs for use in processing  
5 is greater than a data read-out margin of a RAM for  
6 use in processing to be tested in said built-in self  
7 test.

1 7. The semiconductor device according to claim 3,  
2 wherein each of said plural RAMs for use in processing  
3 (further) comprises an extending circuit for  
4 extending a pre-charge release period.

1 8. The semiconductor device according to claim 4,  
2 wherein each of said plural RAMs for use in processing  
3 (further) comprises an extending circuit for  
4 extending a pre-charge release period.

1 9. The semiconductor device according to claim 5,  
2 wherein each of said plural RAMs for use in processing  
3 (further) comprises an extending circuit for  
4 extending a pre-charge release period.

1 10. The semiconductor device according to claim 6,  
2 wherein each of said plural RAMs for use in processing  
3 (further) comprises an extending circuit for  
4 extending a pre-charge release period.

1 11. The semiconductor device according to claim 3,  
2 wherein each of said plural RAMs for use in processing  
3 further comprises an extending circuit for extending  
4 a word selection period.

1 12. The semiconductor device according to claim 4,  
2 wherein each of said plural RAMs for use in processing  
3 further comprises an extending circuit for extending  
4 a word selection period.

1 13. The semiconductor device according to claim 5,  
2 wherein each of said plural RAMs for use in processing  
3 further comprises an extending circuit for extending  
4 a word selection period.

1 14. The semiconductor device according to claim 6,  
2 wherein each of said plural RAMs for use in processing  
3 further comprises an extending circuit for extending  
4 a word selection period.

1 15. The semiconductor device according to claim 7,  
2 wherein each of said plural RAMs for use in processing  
3 further comprises an extending circuit for extending  
4 a word selection period.

1 16. The semiconductor device according to claim 8,  
2 wherein each of said plural RAMs for use in processing

3 further comprises an extending circuit for extending  
4 a word selection period.

1 17. The semiconductor device according to claim 9,  
2 wherein each of said plural RAMs for use in processing  
3 further comprises an extending circuit for extending  
4 a word selection period.

1 18. The semiconductor device according to claim 10,  
2 wherein each of said plural RAMs for use in processing  
3 further comprises an extending circuit for extending  
4 a word selection period.

1 19. A testing apparatus built in a semiconductor  
2 device comprising a RAM for use in processing  
3 incorporated in a data processing system and to be  
4 tested, said testing apparatus comprising:

5 a built-in self test circuit for making a  
6 built-in self test on said RAM for use in processing;  
7 and

8 a RAM for tester for storing results of said  
9 built-in self test on said RAM for use in processing  
10 made by said built-in self test circuit so that the  
11 results of said built-in self test can be read out by  
12 an external tester;

13 a RAM having a data read-out margin greater  
14 than a data read-out margin of said RAM for use in

15    processing being used as said RAM for tester.

1    20. A testing apparatus built in a semiconductor  
2    device comprising a plurality of RAMs for use in  
3    processing incorporated in a data processing system  
4    and to be tested, said testing apparatus comprising:

5            a built-in self test circuit for making a  
6    built-in self test on said plural RAMs for use in  
7    processing;

8            when said built-in self test circuit makes  
9    the built-in self test on a part of said plural RAMs  
10   for use in processing, a RAM for use in processing,  
11   which is not to be tested in said built-in self test,  
12   being used as a RAM for tester which stores results  
13   of said built-in self test on said RAM(s) for use in  
14   processing made by said built-in self test circuit so  
15   that the results of said built-in self test can be read  
16   out by an external tester.

1    21. The testing apparatus for a semiconductor device  
2    according to claim 20, wherein each of said plural RAMs  
3    for use in processing comprises a margin widening  
4    means for increasing a bit line amplitude at the time  
5    of a start of a sense amplifier of said RAM to widen  
6    a data read-out margin.

1    22. The testing apparatus for a semiconductor device

2 according to claim 21, wherein said margin widening  
3 means comprises a delay circuit for gradually delaying  
4 a start timing of said sense amplifier according to  
5 a signal fed from the outside.

1 23. The testing apparatus for a semiconductor device  
2 according to claim 21, wherein said margin widening  
3 means changes a setting so that a data read-out margin  
4 of a RAM used as a RAM for tester among said plural  
5 RAMs for use in processing is greater than a data  
6 read-out margin of a RAM for use in processing to be  
7 tested in said built-in self test.

1 24. The testing apparatus for a semiconductor device  
2 according to claim 22, wherein said margin widening  
3 means changes a setting so that a data read-out margin  
4 of a RAM used as a RAM for tester among said plural  
5 RAMs for use in processing is greater than a data  
6 read-out margin of a RAM for use in processing to be  
7 tested in said built-in self test.

1 25. The testing apparatus for a semiconductor device  
2 according to claim 21, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a pre-charge release period.

1 26. The testing apparatus for a semiconductor device

2 according to claim 22, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a pre-charge release period.

1 27. The testing apparatus for a semiconductor device  
2 according to claim 23, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a pre-charge release period.

1 28. The testing apparatus for a semiconductor device  
2 according to claim 24, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a pre-charge release period.

1 29. The testing apparatus for a semiconductor device  
2 according to claim 21, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a word line selection period.

1 30. The testing apparatus for a semiconductor device  
2 according to claim 22, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a word line selection period.

1 31. The testing apparatus for a semiconductor device  
2 according to claim 23, wherein each of said plural RAMs  
3 for use in processing further comprises an extending



4 circuit for extending a word line selection period.

1 32. The testing apparatus for a semiconductor device  
2 according to claim 24, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a word line selection period.

1 33. The testing apparatus for a semiconductor device  
2 according to claim 25, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a word line selection period.

1 34. The testing apparatus for a semiconductor device  
2 according to claim 26, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a word line selection period.

1 35. The testing apparatus for a semiconductor device  
2 according to claim 27, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a word line selection period.

1 36. The testing apparatus for a semiconductor device  
2 according to claim 28, wherein each of said plural RAMs  
3 for use in processing further comprises an extending  
4 circuit for extending a word line selection period.